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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/777,012	02/11/2004	Richard W. Foote	P05792	3404

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EXAMINER	
FULK, STEVEN J	
ART UNIT	PAPER NUMBER
2891	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/10/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/777,012	FOOTE ET AL.	
	Examiner	Art Unit	
	Steven J. Fulk	2891	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 October 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,7-10,13-17 and 20-42* is/are pending in the application.

4a) Of the above claim(s) *22-42* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,7-10,13-17,20 and 21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 July 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. Applicant's amendment filed October 23, 2006, has been entered. Claims 1-4, 7-10, 13-17 and 20-21 are currently pending.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-3, 7-9, 13-17 and 21 are rejected under 35 U.S.C. 102(b) as being anticipated by Sachitano et al. '640. Where product-by-process limitations are recited, the claims are limited only by the structure implied by the steps, not the manipulations of the steps. For example, anticipation of claim 7 does not require that the doping be performed by implantation (in-situ doping would result in the same structure); anticipation of claim 7, 13, or 16 does not require the doping to be performed simultaneously; anticipation of claim 17 does not require etching to separate the source and drain (masked deposition would result in the same structure).

Regarding claim 1, Sachitano et al. discloses a semiconductor apparatus comprising a double-poly bipolar transistor (fig. 12, 114) and a double-poly metal oxide semiconductor (MOS) transistor (120), wherein a base of the double-poly bipolar transistor (140) and a gate of the double-poly MOS transistor (148) contain substantially identical dopants (both NPN and PNP devices are disclosed; col. 1,

lines 63-66. PNP devices would inherently have an n-type base, which is substantially identical to the n-type dopant of the MOS gate 148).

Regarding claim 2, the reference further discloses the double-poly bipolar transistor and the double-poly MOS transistor to comprise a substrate (fig. 12, 122) and a first layer of polysilicon, Poly1, wherein the Poly1 material in the double-poly bipolar transistor is doped with impurity ions to form an extrinsic base (140) and the Poly1 material in the double-poly MOS transistor is doped with impurity ions to form a MOS transistor gate (148).

Regarding claim 3, the reference further discloses the double-poly bipolar transistor to be a PNP transistor (col. 1, lines 63-66) and the double-poly MOS transistor to be NMOS transistor (fig. 12, 120).

Regarding claims 7 and 8, the substrate is implanted with impurity ions to form an intrinsic base (fig. 4, 150) in the double-poly bipolar transistor and a self-aligned, lightly doped drain in the double-poly MOS transistor (fig. 4, 156 & 158).

Regarding claim 9, the reference further discloses the double-poly bipolar transistor to be a PNP transistor (col. 1, lines 63-66) and the double-poly MOS transistor to be NMOS transistor (fig. 12, 120).

Regarding claims 13-15 and 17, the reference discloses the double-poly bipolar transistor and the double-poly MOS transistor to further comprise a second layer of polysilicon (Poly2) material, wherein the Poly2 material in the double-poly bipolar transistor is doped with impurity ions to form an emitter (fig. 12, 166) that is self-aligned to the extrinsic base and the Poly2 material in the double-poly MOS

transistor is doped with impurity ions to form a separated MOS source/drain (170A & 170B) that is self-aligned to the gate.

Regarding claim 16, the reference further discloses the Poly2 material in the double-poly bipolar transistor to be doped with impurity ions to form a deep collector (fig. 12, 142).

Regarding claim 21, the reference further discloses the double-poly bipolar transistor to be a PNP transistor (col. 1, lines 63-66) and the double-poly MOS transistor to be an NMOS transistor (fig. 12, 120).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 4, 10 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sachitano et al. '640 in view of Suda '441.

Sachitano et al. discloses all of the elements of the claims as discussed in paragraph 3 above, and also discloses a semiconductor apparatus wherein the double-poly bipolar transistor is an NPN transistor (fig. 12, 114) and the double-poly MOS transistor is a PMOS transistor (fig. 12, 118). However, Sachitano et al. does not explicitly teach the base of the NPN transistor and the gate of the PMOS transistor have substantially identical dopants.

Suda '441 teaches a BiCMOS device where the base of an NPN bipolar transistor and the gate of a PMOS transistor to contain the substantially identical P-type dopant of boron (col. 8, lines 14-17; col. 9, lines 59-65).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the P-type transistor gate of the PMOS device of Suda in the BiCMOS process of Sachitano et al. One would have been motivated to do this because Suda taught that P-type gates and N-type gates were art recognized functional equivalents for forming the conductive gate of a PMOS transistor (col. 9, lines 57-65) (MPEP § 2144.06).

Response to Arguments

6. Applicant's arguments with respect to the rejection of claims 1-3, 7-9, 13-17 and 21 under 35 U.S.C. 102(a) have been fully considered but are not found persuasive. Applicant argues that Sachitano does not teach or suggest that a base of the double poly bipolar transistor and a gate of the double poly metal oxide semiconductor contain substantially identical dopants. However, Applicant agrees that Sachitano teaches both the base of a double poly PNP transistor and the gate of a double poly NMOS transistor to have an n-type dopant. The limitation of "substantially identical" found in claim 1 is written broadly enough to be anticipated by both the base and gate containing an n-type dopant (as opposed to one containing a p-type dopant and one containing an n-type dopant). Neither the species of n-type dopant nor the concentration of n-type dopant are required by the claim.

7. Applicant's arguments with respect to the rejection of claims 4, 10 and 20 under 35 U.S.C. 103(a) have been fully considered but are not found persuasive.

Applicant argues that Suda does not teach a PMOS transistor gate and an NPN bipolar transistor to contain substantially identical dopants. However, Applicant agrees that Suda teaches both the PMOS transistor gate and the NPN bipolar transistor to contain a p-type dopant of boron. The limitation of "substantially identical" is written broadly enough to be anticipated by both the base and gate containing a p-type dopant of boron. The concentration of p-type dopant is not required by the claim.

Applicant also argues that there is no suggestion to combine the references. The examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, the motivation to combine is found in both the prior art and in the knowledge generally available to one of ordinary skill in the art, that is P-type gates and N-type gates were art recognized functional equivalents for forming the conductive gate of a PMOS transistor (Suda, col. 9, lines 57-65) (MPEP § 2144.06).

Conclusion

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven J. Fulk whose telephone number is (571) 272-8323. The examiner can normally be reached on Monday through Friday, 9:00am to 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bill Baumeister can be reached on (571) 272-1722. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

10. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

SJF

Steven J. Fulk
Patent Examiner
Art Unit 2891

January 3, 2007

B. WILLIAM BAUMEISTER
SUPERVISORY PATENT EXAMINER
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